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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,615	04/14/2004	Yasuyuki Kudo	500.40682CX1	5092

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-3873

EXAMINER	
WU, XIAO MIN	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/823,615	KUDO ET AL.	
	Examiner	Art Unit	
	XIAO M. WU	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/960,409.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/14/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-20 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-37 of U.S. Patent No. 6,753,880. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-20 are broadening from claims 1-37. The representative claim 1 of the US Patent 6,753,880 and the representative claim 14 of the instant application are compared as follow:

Claim 1of the US Patent No. 6,753,880	Claim 14 of the instant application
1. A display driving device for applying a gray-scale voltage according to display data to a pixel section of a display panel, said display driving device comprising:	14: A display device for displaying display data, comprising: a display panel having pixel sections arranged in a matrix form; a scanning circuit for selecting a line of the pixel sections;
a display memory for storing said display data;	

a histogram memory for storing a frequency of each of said gray-scale voltages with respect to a plurality of pixel sections;	
a gray-scale voltage generation circuit for generating a plurality of gray-scale voltages based on reference voltages; and	a gray-scale voltage generation circuit for generating a plurality of gray-scale voltages based on reference voltages; and
a selection circuit for selecting a gray-scale voltage to be applied to each of said plurality of pixel sections, from said plurality of gray-scale voltages	a selection circuit for selecting a gray-scale voltage to be applied to each of the pixel sections, from the plurality of gray-scale voltages,
wherein said gray-scale voltage generation circuit includes a plurality of voltage generating circuits for generating respective gray-scale voltages; and	wherein the gray-scale voltage generation circuit includes a plurality of voltage generating circuits for generating respective gray-scale voltages; and
wherein a quantity of current of each of said voltage generating circuits is changed according to a frequency of a corresponding gray-scale voltage.	wherein a quantity of current of each of the voltage generating circuits is changed according to a frequency of a corresponding gray-scale voltage.

From the side-by-side comparison above, it is noted that claim 14 of the instant application is broadening from claim 1 of the US Patent No. 6,753,880 since claim 14 does not require the limitation of "a display memory for storing said display data; a histogram memory for storing a frequency of each of said gray-scale voltages with respect to a plurality of pixel sections" as recited in claim 1 of the US Patent No. 6,753,880. It would have been obvious to delete the element display memory and the histogram memory from the claim 14 since the pixel data can be received from other analog data source instead of digital data source stored in the memory.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isami et al. (US Patent No. 6,166,725) in view of Yokouchi et al. (US Patent No. 5,323,171).

As to claims 1, 12 and 13, Isami discloses a display device for displaying display data, comprising: a display panel having pixel sections arranged in a matrix form; a scanning circuit which selects a line of the pixel sections (see Fig. 4); a gray-scale voltage generation circuit (551, Fig. 19) which generates a plurality of gray-scale voltages (e.g. 64 levels of grayscale voltage) based on reference voltages (e.g. nine gray scale reference voltage (V0-V8; see col. 5, lines 55-60); and a selection circuit (561, Fig. 19) which selects a gray-scale voltage corresponding to the display data from the plurality of gray-scale voltages (see col. 6, lines 26-33), and outputs a selected gray-scale voltage to a pixel section of the display panel (577). It is noted that Isami does not current values of the gray-scale voltage generation circuit are changed according to a load of the display panel. Yokouchi is cited tot each a liquid crystal display device similar to Isami. Yokouchi further discloses current values of the gray-scale voltage generation circuit are

changed according to a load of the display panel (see Fig. 1 and col. 4, lines 34-45). It would have been obvious to one of ordinary skill in the art to have modified Isami with the features of load detection as taught by Yokouchi because Yokouchi provides a method of driving the load stably regardless of the change of the source voltage (col. 2, lines 59-61).

As to claim 2,Yokouchi discloses current values of the gray-scale voltage generation circuit become larger as the load of the display panel becomes larger (see col. 4, lines 40-45).

6. Claims 14 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isami et al. (US Patent No. 6,166,725) in view of Cuciurean-Zapan et al. (US Patent No. 6,343,159).

As to claim 14, Isami disclose a display device for displaying display data, comprising: a display panel having pixel sections arranged in a matrix form; a scanning circuit for selecting a line of the pixel sections (see Fig. 4); a gray-scale voltage generation circuit (551, Fig. 19) for generating a plurality of gray-scale voltages (e.g. 64 levels of grayscale voltage) based on reference voltages (e.g. nine gray scale reference voltage (V0-V8; see col. 5, lines 55-60); and a selection circuit (561, Fig. 19) for selecting a gray-scale voltage to be applied to each of the pixel sections, from the plurality of gray-scale voltages, wherein the gray-scale voltage generation circuit includes a plurality of voltage generating circuits (e.g. voltage dividers for 64 grayscale level) for generating respective gray-scale voltages. It is noted that Isami does not disclose a quantity of current of each of the voltage generating circuits is changed according to a frequency of a corresponding gray-scale voltage. Cuciurean-Zapan is cited to teach a display device with a gray scale generation device similar to Isami. Cuciurean-Zapan further discloses disclose a quantity of current of each of the voltage generating circuits is changed according to a frequency

of a corresponding gray-scale voltage (see col. 8, lines 5-12 and 18-24). It would have been obvious to one of ordinary skill in the art the art to have modified Isami with the features of the frequency of a corresponding gray-scale voltage as taught by Cuciurean-Zapan because Cuciurean-Zapan provides improved systems and methods that model and reconstruct grayscale images from halftone images (col. 3, lines 21-23).

As to claims 16-18, Isami discloses the gray-scale voltage generation circuit (551) comprises a divider which is equivalent to buffer circuits for converting impedances of the reference voltages. It would have been obvious that the output quantity of current of each of the buffer circuits becomes larger as the frequency of the corresponding gray-scale voltage becomes large because the current is changed in accordance with the frequency of the corresponding gray-scale voltage.

As to claim 19, Isami discloses that the gray-scale voltage generation circuit makes a quantity of current of each of the voltage generating circuits large during a first interval in one scanning interval for applying the gray-scale voltages every the pixels sections to said display panel, and makes a quantity of current of each of the voltage generating circuits small during a second interval in said one scanning interval (see col. 18, lines 5-25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE, can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.

March 19, 2006

XIAO M. WU
Primary Examiner
Art Unit 2629